Applications of Transformation Techniques in CDMA Receivers

Ramin Baghaie
Helsinki University of Technology
Laboratory of Telecommunications Technology
P.O. BOX 3000, FIN-02015 HUT, Finland
e-mail: ramin.baghaie@hut.fi

***Abstract*- This paper discusses the application of different algorithm transformation techniques in Code Division Multiple Access receivers (CDMA). This is achieved by looking at some of the computational blocks that constitute the CDMA receivers. We focus on the Look-Ahead, Relaxed Look-ahead and Strength Reduction algorithm transformation techniques and demonstrate how CDMA receivers could benefit when utilizing these techniques during the course of implementation.**

I. INTRODUCTION

Currently, enormous research has been carried out into the application of Wideband Code Division Multiple Access (WCDMA) scheme as an air interface for Universal Mobile Telecommunications Systems (UMTS). One of the main features of the UMTS is to provide a variety of services such as multimedia [1]. However, services such as video telephony and multimedia demand higher data rates.

In order to achieve higher processing speed pipelining and parallel processing approaches can be utilized. On the other hand, when dealing with the implementation of mobile systems, the pipeline approach could be more desirable due to its lower hardware cost.

Further more, the need for smaller handsets is evident. Batteries play a major role in the weight and size of handsets and these in turn are directly impacted by the power dissipated by the electronic circuits. Thus, in the course of implementation, in order to satisfy the enforced higher data rates and lower power consumption constraints of the wireless communication systems such as UMTS, alternative methods such as algorithm transformation techniques should be taken into considerations.

In this paper, we focus on some of these transformation techniques and demonstrate their importance when implementation of CDMA receivers is of interest. This paper is organized as follows. Section II studies the Look-Ahead (LA), Relaxed Look-ahead (RLA), and Strength Reduction (SR) transformation techniques. In Section III, we demonstrate how CDMA receivers can benefit when utilizing these techniques during the course of implementation. A summary is provided in Section IV.

II. TRANSFORMATION TECHNIQUES

Transformations can be divided into two main categories: architectural transformations that can be used to design families of architectures for a given algorithm, and algorithm transformations that target the algorithm structure of various algorithms [2]. By utilizing transformations it is possible to explore a number of alternative structures and to choose those that result in a higher throughput, lower power consumption or a combination of both. In the following sections, we briefly describe three algorithm transformation techniques.

A. The Look-Ahead and Relaxed Look-Ahead Techniques

Pipelined DSP algorithms allow us to tradeoff speed, power and area during the course of VLSI implementation. Pipelining is simply accomplished by placing latches at any feed-forward cutsets of the data flow graph representation of the algorithm. Although applying pipelining to algorithms without feedback is rather simple, pipelining of DSP algorithms having a feedback loop is not trivial. Inserting latches to pipeline the recursive loop of such algorithms is only useful, when execution of multiple interleaved independent data is of interest. This however, will not improve the iteration bound of such algorithms [2]. As a result, algorithm transformation techniques such as the Look-Ahead and the Relaxed Look-Ahead have been proposed for pipelining of recursive DSP algorithms [2].

In the LA technique, the algorithm of interest is iterated as many times as desired to create the required level of concurrency. In other words, in order to create a M stage pipeline, the first order state $x(n)$ is iterated until expressed as $x(n\text{-}M)$. The application of LA technique, however, results in a large hardware overhead and in many cases due to this large overhead the resulting systems are not practical for the Application Specific Integrated Circuit (ASIC) implementations [2].

On the other hand, the Relaxed Look-Ahead technique approximates the algorithms that are obtained via the look-ahead technique. Depending on the approximations, the hardware overhead can be very small, however this maybe in expense of some performance degradation [2]. In Section III, we will demonstrate that in many applications, this degradation is rather negligible. As a result, the pipelined architectures will operate M times faster and this increased of throughput can be exchanged for either reducing power or chip area.

B. The Strength Reduction Technique

In this section, we briefly describe the SR transformation. The SR technique reduces the hardware complexity by exploiting

substructure sharing. This is done by reducing the number of more complex operations such as multiplications at the expense of increasing the number of simpler operations such as additions. Thus, by utilizing the SR the power consumption or the silicon area can be reduced [2]. As an example, consider the problem of computing the product of two complex numbers *A* and *B*:

$$C = AB = (A_R + jA_I)(B_R + jB_I) \tag{1a}$$

$$C = (A_R B_R - A_I B_I) + j(A_R B_I + A_I B_R) \tag{1b}$$

The direct implementation of (1) requires a total of four real multiplications and two real additions. However, by applying the SR transformation we can reformulate Equation (1) as:

$$C_R = (A_R - A_I)B_I + A_R(B_R - B_I) \tag{2a}$$

$$C_I = (A_R - A_I)B_I + A_I(B_R + B_I) \tag{2b}$$

As can be seen from (2a) and (2b), by using the SR transformation total number of real multiplications is reduced to only three. This however is at the expense of having three additional adders (see Fig. 1). It is important to note that by means of linear transformation it can be proved that for the realization of (2) the structure of Fig. 1b is not unique and other structures exist. In fact in [3], sixteen different realizations of (2) and their noise properties were reported.

The switching or the dynamic power dissipation of a CMOS circuit mainly depends on the number of logic transitions per unit time. Now, let us assume that on average, the number of logic transitions required for one multiplication is N_a times that of one addition. Thus, the power reduction (*PR*) due to the SR transformation can then be estimated as follows:

$$PR = \frac{P_{normal} - P_{SR}}{P_{normal}} \tag{3}$$

By inserting $P_{normal} = (4N_a + 2)$ and $P_{SR} = (3N_a + 5)$ into (3) we have:

$$PR = \frac{N_a - 3}{4N_a + 2} \tag{4}$$

Therefore, for a single complex multiplication of (1) power reduction of up to 25% can be achieved.

Furthermore, as an example consider a 16-bit multiplier. Based on the required number of gates, one 16-bit multiplier requires at least 10 times the area of one 16-bit adder [4]. Thus, as a result of the SR transformation in addition to power savings, more than 16% of area reductions can be achieved. By observing Fig. 1, it is easily seen that the application of the SR transformation increases the computation time of the critical path. This may be undesirable in some applications. However, by utilizing the pipelining schemes such as the LA and the RLA this problem can be eliminated.

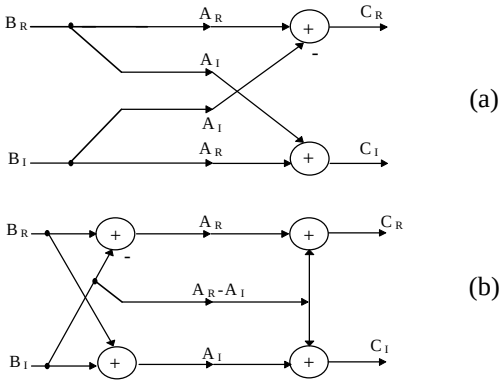

Fig. 1. Realization of a) direct structure of (1) b) using the SR transformation of (2) [3]

III. TRANSFORMATION TECHNIQUES IN CDMA

In this section, we demonstrate how CDMA receivers can benefit when utilizing these techniques during the course of implementation.

A. Application of Relaxed Look-Ahead Technique in Adaptive CDMA Receivers

In the Direct Sequence CDMA (DS-CDMA) receivers, in order to suppress the Multiple Access Interference (MAI) different multiuser detectors such as the Minimum-Mean-Square-Error (MMSE) receiver can be utilized [5,6]. In such receivers, different adaptive schemes can be applied. Consequently, by utilizing adaptive algorithms, receivers become less sensitive to the interfering powers. As a result, there will be room for more users as compared to the matched filter solution.

In this section, we investigate the implementation of adaptive receivers by utilizing the RLA technique. As an example, consider an adaptive Multiple-Antenna CDMA receiver. In Fig. 2, the structure of a typical linear adaptive receiver equipped with *N* antennas is illustrated. In this receiver, each of the *N* antenna branches contains a linear filter whose coefficients are to be optimized. The filtered signals from each antenna are then added together to form a decision variable. In Fig. 2, r_i denotes the received signal after chip-matched filtering at antenna *i*, $\mathbf{h}_i$ contains the complex filter coefficients for the *i*th antenna. The decision variable *z*, can be written as follows:

$$z = \mathbf{h}^{\mathrm{H}}\mathbf{r} \tag{5}$$

The goal is to find filter $\mathbf{h}$ such that the output *z* is minimized under the constraints that the desired user's code sequence in every antenna can pass undistorted [7,8].

For the ease of implementation, by utilizing the structure of the generalized sidelobe canceler, the weight vector $\mathbf{h}$ can be decomposed into two parts as:

$$\mathbf{h} = \mathbf{h}_q - \mathbf{C}_a\mathbf{h}_a \tag{6}$$

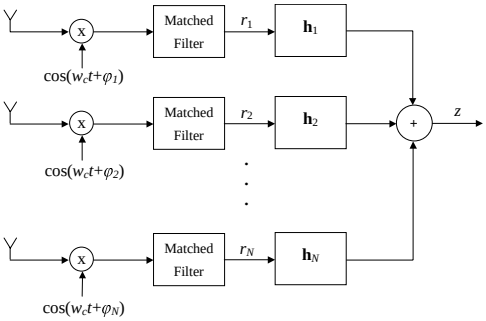

Fig. 2. Structure of an adaptive multiple-antenna receiver

where $\mathbf{h}_q$ is a fixed vector satisfying the constraint equations, and $\mathbf{h}_a$ is an adaptive filter. For a more detailed derivation of this system the interested reader may refer to [7,8].

For the implementation of the adaptive filter $\mathbf{h}_a$, different algorithms such as the Least Mean Squares (LMS) or the Recursive Least Squares (RLS) can be utilized [9]. Despite the simplicity of the LMS algorithm, its convergence speed is rather slow as compared to the RLS algorithm. This can not be tolerated in many applications and mobile communications is of no exception.

In [7,8], pipelined implementation of the multiple-antennas adaptive mobile receivers were investigated. For the pipelined implementation of these receivers, the RLA technique was utilized. Table I provides a comparison between two implementation techniques.

TABLE I
COMPARISON BETWEEN TWO IMPLEMENTATION TECHNIQUES

	Adders	**Latches**	**Convergence rate**	**Misadjustment**
RLA-LMS	*M*-1	2(*M*-1)	fixed	*M* dependent
RLA-RLS	-	2(*M*-1)	*M* dependent	No

As can be seen from Figures 3, 4 and 5, as the number of pipelining stages *M* increases, the signal-to-interference ratio (SIR) will decrease. In the LMS case, this is due to the higher misadjustment as a result of the RLA approximations (see Fig. 3). In the RLS case, the convergence speed is *M* times slower. However, one can stop the updating process after a certain number of iterations. This however, will cause the decrease of SIR in the RLS case. As an example, in Figures 4 and 5, the updating of the coefficient vectors were stopped after 300 and 500 iterations (*I*), respectively. The numerical results in [7,8] illustrated that for a moderate *M* the performance loss is rather small.

As a result, by applying these techniques the pipelined architectures will operate *M* times faster. Thus, in the cases where the original throughput is sufficient, this increased of throughput can be exchanged for either reducing power or chip area.

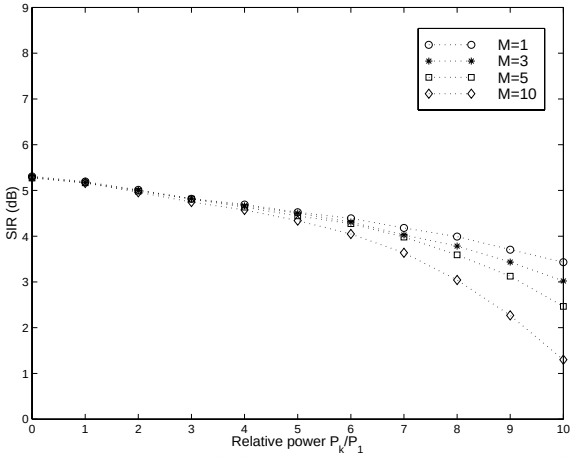

Fig. 3. SIR versus the relative powers of the interfering users using one antenna (LMS case) [8]

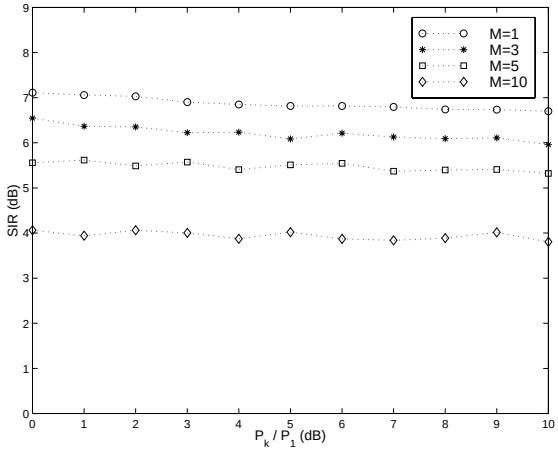

Fig. 4. SIR versus the relative powers of the interfering users using two antennas and *I*=300 (RLS case) [7]

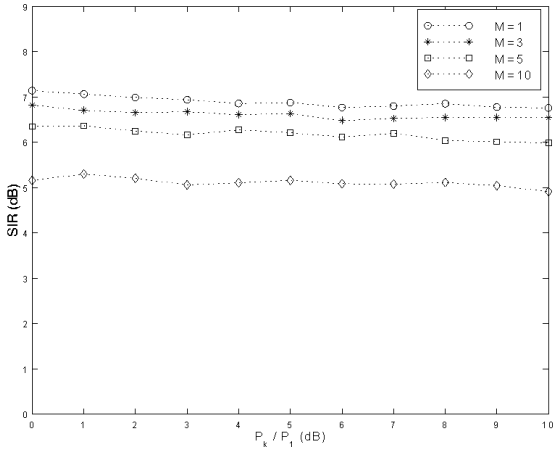

Fig. 5. SIR versus the relative powers of the interfering users using two antennas and *I*=500 (RLS case) [7]

B. *Application of Strength Reduction Technique in RAKE Receivers*

The conventional CDMA receiver in the case of a multipath fading channel consists of a bank of RAKE receivers, one for each active user at the base station. Some form of RAKE structure at the receiver front-end can be used in both single-user and multi-user CDMA receivers [10]. A RAKE receiver collects the signal energy from different multipath components. The optimal RAKE receiver actually implements a channel matched filter which maximizes the received signal-to-noise ratio [11]. Although direct implementation of RAKE receivers seems to be trivial and straightforward, the following issues should be considered. Consider a tapped delayed line channel model with L taps [11]. This will correspond to having L fingers in the RAKE receiver of Figure 6. Thus, for the implementation of this receiver L complex multipliers are needed. In the multiuser CDMA systems, for every active user one RAKE receiver is needed. Considering K users for every base station and L paths, a minimum of KL complex multipliers or $4KL$ real multipliers are needed. The situation will be even more severe when dealing with Multiple-Antenna CDMA systems. By taking into account some typical values for K = 30-50 and L = 3-5, one can see that up to 90-250 fingers or complex multipliers are needed. In [12], a typical block diagram of a RAKE finger is given. This structure is very similar to the ones reported in other publications. The core of the above mentioned finger is actually the complex multiplier of Fig. 1a. From the implementation point of view, the complex multipliers of the RAKE fingers are the dominant part of the power consumption in the RAKE receiver. Therefore, by applying the SR technique to the fingers of RAKE receiver of Fig. 2b, remarkable savings in consumed power and silicon area can be achieved. Thus, as a result of the application of the Strength Reduction transformation in RAKE receivers, noticeable power and area reductions can be achieved [4]. It is important to note that the concept of the SR transformation can be applied to any other blocks of telecommunication systems that are dealing with complex multiplications.

IV. Summary

This paper addressed the application of efficient algorithm transformation techniques in CDMA receivers. By applying these techniques in the course of implementation, one can achieve higher throughput, lower power consumption, lower chip area or a combination of all the mentioned factors. To conclude, we hope that with the aid of this overview, we have managed to demonstrate the importance and relevance of the algorithm transformation techniques in telecommunication systems such as UMTS.

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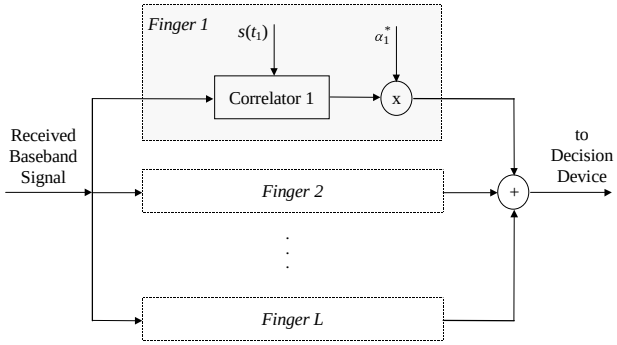

Fig. 6. Typical structure of a RAKE receiver

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