IMPLEMENTATION OF LOW-POWER CDMA RAKE RECEIVERS USING STRENGTH REDUCTION TRANSFORMATION

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ABSTRACT

In a Code Division Multiple Access system operating in a multipath fading channel, a bank of RAKE receivers is needed for each active user at the base station. In this paper, low-power RAKE receivers are proposed that utilize the Strength Reduction (SR) transformation technique. The SR transformation can result in remarkable savings in consumed power and silicon area. A possible disadvantage of the SR transformation is that it increases the computation time of the critical path. However, this problem can be alleviated by different pipelining schemes.

1. INTRODUCTION

Fading and multipath propagation is a major problem in radio communication systems. Code Division Multiple Access (CDMA) systems are no exception to this phenomenon. Wideband spread-spectrum signals are subject to frequency-selective fading. However, multipath propagation also provides a form of diversity and can thus be used to combat the effects of fading [1]. CDMA systems can take advantage of this factor by using a RAKE receiver which collects the signal components from different paths and combines them [2,3]. A RAKE processing unit is a basic component not only in conventional single-user CDMA receivers but also in more dedicated optimal or suboptimal multiuser receivers [4].

On the other hand, wireless devices are rapidly making their way to the market and the desirability of wireless communications and portable operations of all types is very clear. It is also a fact that batteries are a major, if not the dominant factor in the weight and size of portable electronic systems and these in turn are directly impacted by the power dissipated by the electronic circuits.

In CMOS, the current dominant VLSI technology, there are three sources of power dissipation: switching, short circuits and leakage currents. The switching component also known as the dynamic power is the most essential one.

The average switching power for a CMOS gate with an average load capacitor C_L is given by [5]:

$$P_{switching} = C_L \cdot V_{dd}^2 \cdot f \quad (1)$$

where f is the clock frequency and V_{dd} is the supply voltage.

From Eq. (1) it is clear that the quadratic influence of voltage on power makes voltage scaling the most attractive scheme for power reduction and thus operating at the lowest possible voltage is most desirable. This often comes at the cost of increased delays and thus reduced throughput. However, by modifying the architecture through appropriate transformations the throughput can be regained and thus a power saving can be accomplished while retaining the required functionality and throughput [5].

Potentially one of the most important techniques involves combining architecture optimization with voltage scaling, which allows a trade-off between silicon area and low power operation. The main idea is to maintain throughput at reduced supply voltages through parallel processing or pipelining. By utilizing parallel architectures, the speed requirements on each unit are reduced, allowing for a reduction in voltage.

Power reduction can also be achieved by other techniques such as selecting various topological choices for implementing a given function [6], choosing an architecture that minimizes the effective switched capacitance at a fixed voltage [5] or utilizing different transformation techniques [5],[7]. Transformations are modifications to the computational structure in a manner that the input-output behavior is preserved. By utilizing transformations it is possible to explore a number of alternative architectures and to choose those which result in the lowest power consumption [5].

In this paper, we investigate the application of one transformation technique, referred to as the *Strength Reduction* (SR) transformation in RAKE receivers. This paper is organized as follows. In Section 2, the structure of RAKE receivers are briefly reviewed. Section 3 deals with the SR transformation. In Section 4, the application of the SR transformation to the RAKE receiver implementation is discussed. Section 5 deals with power and area reductions as a result of the SR transformation. Finally, conclusions are drawn in the last section.

2. RAKE RECEIVER

The conventional CDMA receiver in the case of a multipath fading channel consists of a bank of RAKE receivers, one for each active user at the base station [8]. Some form of RAKE structure at the receiver front-end can be used in both single-user and multi-user CDMA receivers.

A RAKE receiver collects the signal energy from different multipath components. The optimal RAKE receiver actually implements a channel matched filter which maximizes the received signal-to-noise ratio. This is also called the maximum ratio combiner [2]. This means that the identified multipath components are weighted proportionally to the amplitude of the component. Of course, the optimal RAKE receiver can only be implemented if the multipath components or the channel's impulse response are known [1,2].

Depending on the speed of the receiver or the characteristics of the channel, i.e. static, slow fading or fast fading, different types of RAKE receiver architectures have been proposed [1,9-17]. However, a detailed comparison and analysis of these techniques are out of the scope of this paper.

A typical RAKE receiver consists of a delay line, taps with complex multipliers and integrators which in a spread-spectrum system are implemented as correlators with the user's spreading code or signature sequence. Figure 1 illustrates the structure of a typical RAKE receiver in which $s(t_k)$ and α_k^* $\{k=1,\ldots,L\}$ represent the user's signature sequence and the complex conjugate estimate of the channel's impulse response, respectively. As the multipath components of the impulse response are usually not evenly spaced, the time spacing between adjacent fingers is not constant.

From the implementation point of view, a major part of the power consumption of the RAKE receiver is caused by the complex multipliers. The main objective of this paper is to develop efficient techniques for the implementation of the complex multipliers of the RAKE receivers. In Section 4, we will discuss some of the implementation issues of such RAKE receivers and propose a structure for a RAKE receiver that has a lower power consumption and requires less silicon area.

3. STRENGTH REDUCTION TRANSFORMATION

In this section we describe the SR transformation. This transformation reduces the power consumption by decreasing the number of operations. This minimizes the effective switched capacitance as was explained earlier in Section 1.

Consider the problem of computing the product of two complex numbers *A* and *B*:

$$C = AB = (A_R + jA_I)(B_R + jB_I)$$
$$C = (A_R B_R - A_I B_I) + j(A_R B_I + A_I B_R) \quad (2)$$

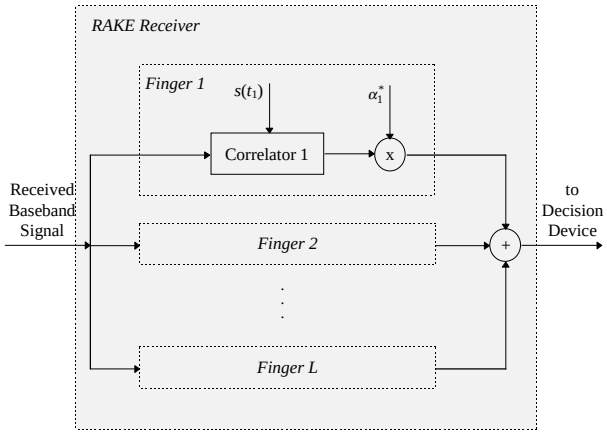

Figure 1. A Typical Structure of a RAKE Receiver

From Equation (2), the direct architectural implementation requires a total of four multiplications and two real additions to compute the complex product. However, by applying the Strength Reduction transformation we can reformulate Equation (2) as:

$$C_R = (A_R - A_I)B_I + A_R(B_R - B_I) \quad (3a)$$
$$C_I = (A_R - A_I)B_I + A_I(B_R + B_I) \quad (3b)$$

As can be seen from Equations (3a) and (3b), by using the SR transformation the total number of real multiplications is reduced to only three. This however is at the expense of having three additional adders (see Figure 2).

The complex multiplications of Eq. (2) can be also written in a matrix form [18,19]. As a result, it is shown that a minimum of three multipliers are needed [19]. It is important to note that by means of linear transformation it can be proved that for the realization of Eq. (3) the structure of Figure 2b is not unique and other structures exist. In [19], sixteen different realizations of Eq. (2) and their noise properties were reported.

By observing Figure 2, it is easily seen that the application of the Strength Reduction transformation increases the computation time of the critical path.

$$T_{critical\_normal} = T_{add} + T_{mult} \quad (4)$$
$$T_{critical\_SR} = 2T_{add} + T_{mult} \quad (5)$$

This may be undesirable in some applications. However, this problem could be combated by different pipelining schemes such as the Look-ahead and relaxed look ahead techniques [20]. As a result of such pipelining techniques, throughput will increase. Now, by considering Eq. (1), one could easily conclude that the increased throughput as a result of pipelining can be exchanged partially for lower power consumption.

It is also well known that multiplications are more complex than additions and consume much more power as well. In [6], dynamic power dissipation, area, and speed of CMOS implementation of various types of adders and multipliers were investigated and compared.

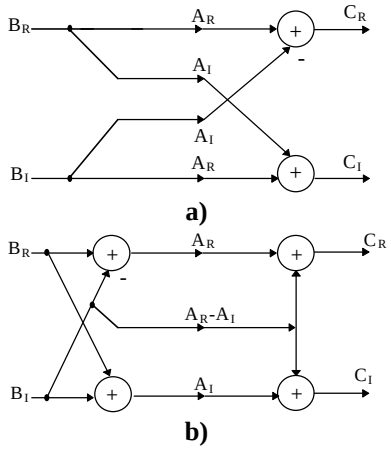

Figure 2. Realization of a) direct structure Eq. (2) b) using the SR transformation Eq. (3)

In these comparisons, it was shown that amongst the compared structures the Carry Lookahead adder was the best choice for word sizes of 16 to 64 bits. As for multipliers, the Wallace and the Dadda structures were the best candidates with word sizes of 8 to 32. In Table 1 some of the features of these circuits for the same word size are compared.

Table 1. Comparison between a typical adder and two multipliers with word lengths of 16 bits

	Carry Lookahead adder	Dadda Multiplier	Wallace Multiplier
Number of gates	200	2477	2569
Average number of logic transitions	100	3389	3874

4. APPLICATION OF THE SR TRANSFORMATION IN RAKE RECEIVERS

Despite the fact that a great deal of research has been done on different types of RAKE receivers, only a few publications have been released that concentrate on the actual implementation of such receivers [9,10,16]. Although direct implementation of RAKE receivers seems to be trivial and straightforward, the following issues should be considered.

Consider a tapped delayed line channel model with L taps [2]. This will correspond to having L fingers in the RAKE receiver of Figure 1. Thus, for the implementation of this receiver L complex multipliers are needed. In the multiuser CDMA systems, as explained in Section 2, for every active user one RAKE receiver is needed. Considering K users for every base station and L paths, a minimum of KL complex multipliers or $4KL$ real multipliers are needed. The situation will be even more severe when dealing with Multiple-Antenna CDMA systems.

By taking into account some typical values for K = 30 -50 and L = 3-5, one can see that up to 90-250 fingers or complex multipliers are needed. In [9], a typical block diagram of a RAKE finger is given. This structure is very similar to the ones reported in [9,10,16]. The core of the above mentioned finger is actually the complex multiplier of Figure 2a. As it was mentioned earlier, from the implementation point of view, the dominant part of the power consumption of the RAKE receiver is caused by the complex multipliers of the RAKE fingers. Therefore, one can conclude that by simply replacing it with the SR multiplier of Fig. 2b, remarkable savings in consumed power and silicon area can be achieved.

5. POWER AND AREA REDUCTIONS

The switching or the dynamic power dissipation of a CMOS circuit mainly depends on the number of logic transitions per unit time. Lets assume that on average, the number of logic transitions required for one multiplication is M times that of one addition. Thus, the power reduction (PR) due to the SR transformation can be estimated as follows:

$$PR = \frac{P_{normal} - P_{SR}}{P_{normal}} \tag{6}$$

Inserting $P_{normal} = (4M + 2)$ and $P_{SR} = (3M + 5)$ we get:

$$PR = \frac{M - 3}{4M + 2} \tag{7}$$

Thus, as a result of the SR transformation, for a single complex multiplication of Eq. (1) power reduction of up to 25% can be achieved. An interesting comparison is to relate the average number of logic transitions of Table 1 with the result of [21]. In [21], it was argued that the effective capacitance of a multiplier is K_c times that of an adder. As an example, it was mentioned that in the case of an array-based multiplier structure, K_c is approximately equal to the number of bits required to present one operand [21]. As an example, based on the figures of Table 1, for a 16-bit Dadda Multiplier, the PR is 22%. In the case of the K_c factor for the same number of bits, the PR corresponds to 20%. Since K_c depends on the word length, special attention should be given to the tradeoff between chip area and system performance, i.e. bit error rate, through careful choice of word lengths for each processing block. In [22] and [23], the influence of quantization on the performance of CDMA receivers has been studied, and it has been shown that word lengths of 4 to 6 bits are sufficient for the baseband signals.

Furthermore, from Table 1 one can conclude that based on the required number of gates, one 16-bit multiplier requires at least 10 times the area of one 16-bit adder. Thus, as a result of the SR transformation in addition to power savings, more than 16% of area reductions can be achieved. As a rule of thumb, as the word length doubles, the required area by one multiplier will be twice as much as that of one adder.

6. CONCLUSIONS

As a result of the application of the Strength Reduction transformation in RAKE receivers, noticeable power and area reductions were achieved. The application of SR transformation increases the critical path computation time. This could be undesirable in some applications. However, this problem can be combated by different pipelining schemes such as the Look-ahead technique.

It is important to note that the concept of the SR transformation can be easily applied to any other blocks of telecommunication systems that are dealing with complex multiplications.

ACKNOWLEDGMENT

This work is part of a research project of the Institute of Radio Communication (IRC) funded by Technology Development Center (TEKES), NOKIA Research Center, Telecom Finland and the Helsinki Telephone Company.

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