EFFICIENT IMPLEMENTATION OF MULTIMEDIA ALGORITHMS ON STANDARD PROCESSORS

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ABSTRACT

Multimedia algorithms are computationally intensive as they require a huge processing power. With the advent of multimedia processors, fast graphics adapters and the evolution of the operating systems, most of these algorithms can be realised in software. As an example for such algorithms, we consider decoding Standard digital TV signals on low end multimedia capable processor such as a Celeron 366Mhz and also High Definition digital TV signals on a fast and powerful processor such as a Pentium IV. The comparision between the Pentium-II,Pentium-III and Pentium IV architecture for multimedia processing is given. The figure 1 shows the simple decoder architecture which is implemented.

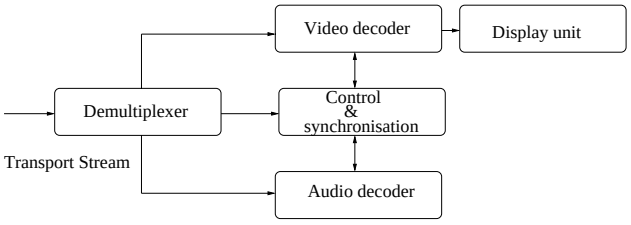

Figure 1. Software decoder architecture

1 Standard definition and High definition digital TV

The digital TV in the either format conforms to MPEG-2 MP@ML or MP@HL (Main Profile at Main Level, Main Profile at High Level) compression scheme respectively. This is based on traditional block based approach employing DCT(Discrete Cosine Transfrom) and motion estimation to remove the redundancy within a frame and also across the frames respectively. The standard definition tv signals are restricted to a maximum frame size of 720x576 for PAL and 720x480 for NTSC with an additional restriction on bitrate going as high as 15 mbps. The High Definition TV signals have a maximum frame size of 1920x1088 and the bitrate starts from 20 mbps. Just comparing the frame sizes for the two standards, we can say that the computation complexity for High Definition TV increases by a factor of five when compared to that of the Standard Definition TV. The internal memory requirements jump from 4MB to 12MB when decoding High Definition TV data. This large requirement on memory and on computation power put some stringent requirements on the processor as well as on the graphics adapter. During our experiments with the High Definition TV data, to achive a real time 30 fps, we would require a transfer of 180 MB/s of raw RGB data from the system memory to the graphics memory. We found that not all the graphics card could handel such large amount of raw data for real time display. Tests were conducted on Linux running latest freely availabel X-Server, using available programs such as DGA(Direct Graphics Access). The graphics card used in the tests were ATI-Radeon and Creative Gforce-2. These requirements will certainly saturate any low end processor.

Bit Rate in Mbps	No of Intra Blocks	No of Non-Intra Blocks
4	279462	1685217
6	308094	1847514
20	1929300	9411275

Comparision of No. of Intra and Non-Intra Blocks

Figure 2. Comparision of No of Blocks

2 Implementation HDTV Decoder

In our implementation of the decoder, the entire process is completely implemented in software on operating systems such as Linux and Windows. The performance of the decoder on these two operating systems for Standard Definition TV data is on par with each other. The transport stream demultiplexer is responsible for demultiplexing the audio and video data from the multiplexed stream. The audio standard used in High Definition TV is Dolby AC3 whose performance and resource requirements are quite small when compared to that of the video and hence it is not reported in this paper. The combined resource requirements for the demultiplexer and the audio decoder is comparitively small to that imposed by the video decoder and the display units combined. This implementation for High Definition TV is on Pentium-IV processor running at 1.4Ghz. The running system is profiled on both Windows and Linux using V-Tune and gprof utilities respectively. The following sections we discuss the various factor affecting the performance of the High Definition TV decoder.

3 Factors affecting the performance

There are many factors which affect the performance of the software only decoder when trying to decode High Definition TV data. They can be broadly classified into processor architecture, clock speed, internal bus architecture, capabilities of the graphics adapters to display High Definition TV and operating system issues. These issues affect the overall performance of the system, especially true in the case of High Definition TV data. The processor architecture, clock speed and the internal bus architecture determine the amount of data that can be pushed to the graphics adapter and the graphics adapter capabilities determine the final throughput of the system.

3.1 Comparison between the processors

Apart form the increase in clock speed from P-III and P-IV there are many architectural differences between the two processors with respect to processing the multimedia data. The additional 144 multimedia instructions available for integer arithmetic on P-IV help in motion compensation routine as we can operate on 128 bits of data at a time. Coupled with 400 Mhz system bus provides a 3.2 GB/s transfer speed between the Pentium-IV processor and the memory controller. With an increased level 2 cache also provides a considerable thourghput.

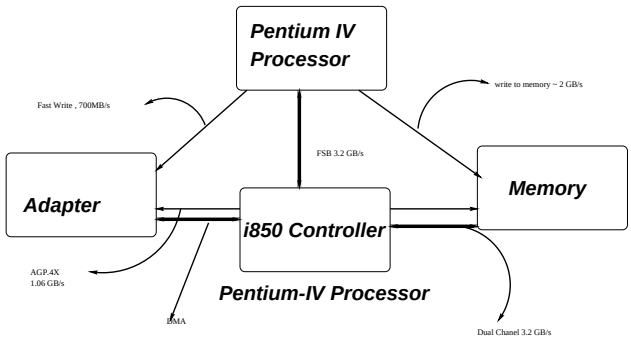

Figure 3. Pentium 4 bus architecture

3.2 Operating Systems Issues

The development tools availabel for implementing the new set of multimedia instructions on Pentium-IV are quite well developed under Windows platform while the same are not yet stabel under Linux. Since the latest multimedia instructions requires the support from the operating system, We have used, not yet stabel compilers and assemblers on the Linux platform to implement the critical loops such as motion compensation and inverse discrete cosine transform(IDCT). Considerabel throughput is achieved in the above critical loops as we can manipulate 128 bits at a time reducing the loops by another factor of two.

4 Performance

The figure show the performance of the software based decoder working at various bitstream speeds. The performance were measured on Standard Definition TV running on Celeron and a Pentium-III processor. The High Definition decoder works at 16.02 fps on a Pentium-IV processor at 1.4Ghz.

5 Future

The theoritical requirement for a full software only HDTV decoding would require a 2GHz processor. Since the processors, especially Pentium-IV are getting faster and faster, we should be abel to decode a fully complaint HDTV streams by the end of this year.

6 References

1. "Digital Video: An Introduction To MPEG-2" Barry G. Haskell, Atul Puri, Arun N. Netravali, Chapman and Hall 1997
2. "Intel Architecture Software Developer's Manual: Instruction Set Reference", http://developer.intel.com
3. "A SoftWare-Based Real-Time MPEG-2 Video Encoder", IEEE Transactions on Ciruits and Systems for Video Technology, Vol 10, No. 7, October 2000

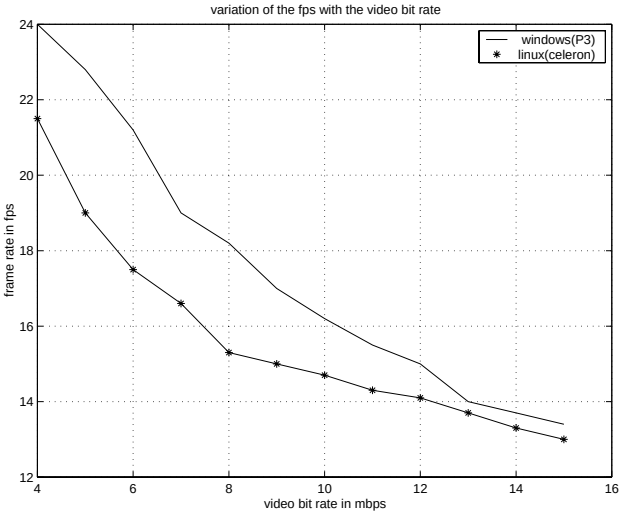

Figure 4. Comparison between Celeron/Pentium-III