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A Dynamic Element Matching Technique for Flash Analog-to-Digital Converters

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ABSTRACT

A flash analog-to-digital converter is proposed that employs a new dynamic element matching architecture. The architecture uses a new strategy of incorporating switches in the voltage reference generator that allows lower hardware complexity and higher conversion speed than comparable converters. The converter has been modeled and simulated on a behavioral level in Matlab. The results indicate good linearity properties that together with the expected speed performance should make it suitable in intended communications applications.

1. INTRODUCTION

Dynamic element matching (DEM) has been used for a couple of decades in digital-to-analog converters (DACs) [1]. It has been used in stand alone DACs as well as DACs used in analog-to-digital converters (ADCs) [2][3][4][5]. More and more of the converter applications are targeted towards communication, where the spectral properties are important. Hence, in the past years some attempts have been made to introduce DEM also in ADCs, thereby improving the spectral properties of the ADC [6][7].

Due to process variations, mismatch errors will be introduced during the manufacturing of the circuits. To compensate for these errors, static and dynamic matching techniques need to be employed. When using static matching, the components are placed close together in certain patterns and made sufficiently large to yield small relative errors. This reduces the variation between the components. Another approach, used in, e.g., current steering DACs is dynamic element matching (DEM) [8]. A current steering DAC consist of a number of current sources, which can be switched on or off. Depending on the digital value of the input signal, a certain number of the currents sources is turned on. Connecting the current sources in series with a resistor generates the output voltage.

Since the geometry of the transistors deviates, which the current sources are constructed from, the current will also deviate. Hence, the step between each output level of the DAC varies, which introduces spurious tones in the output. If DEM is used the current sources to turn on is chosen randomly each sample, causing the frequency domain distortion to be spread out over the frequency range as approximate white noise. Hence, the spurious tones are removed, but the noise floor is raised. This can be compensated for by applying oversampling, thereby getting a higher SFDR compared with not using DEM [8].

Concerning prior use of DEM in ADCs, DEM is introduced in a pipelined ADC in [9]. In [7] and [10] the introduction of DEM in the voltage reference generator of a flash ADC is presented. The latter is accomplished by adding a number of switches between each adjacent resistor in the reference generator. Hence, the voltage on each output of the reference generator can be changed during operation. A certain comparator will thereby compare different input levels in different sample instances. If the switches are connected to a random generator, which updates the reference voltages each sample, the uncertainties in resistor values, as well as offset voltage of the comparators will generate less spurious tones in the output. Hence, it is the same effect as when using DEM in DACs. The drawback with the solutions in [7] and [10] is that the circuits only work for low frequency applications due to the parasitics associated with actual switches. However, if the ADC is to be used in, e.g., communication applications, it must be able to operate at higher frequencies. Here we present a solution with less complexity that can operate at higher frequencies than in [7] and [10]. This makes it more suitable for, e.g., communication applications.

In the following, some of the error sources in flash ADCs are discussed, and a DEM technique aimed at reducing their effect on the output is proposed. The architecture presented in [7] is explained and we present our DEM flash ADC architecture. It has been modeled in Matlab and the results are presented along with the conclusions.

2. ERROR SOURCES IN FLASH ADC

In a flash ADC (illustrated in Figure 1) the input signal is applied to the inputs of $2^N - 1$ comparators, where N is the number of bits. Each comparator is connected to a reference voltage, commonly generated by a resitor ladder.

The output of a comparator is one if the input signal is larger than the reference level connected to the comparator and zero otherwise. The output of the comparators is then decoded to, e.g., binary code. This can be done in different ways. One approach is described in [11] and [12], where the binary output of the decoder is obtained by counting the number of ones on the outputs of the comparators.

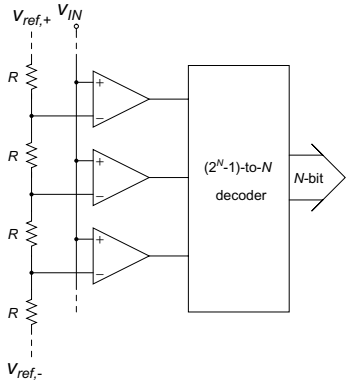


Figure 1: Illustration of flash analog-to-digital converter.

Due to mismatch, the resistance values deviate from the nominal values. Hence, the reference levels deviate from the nominal levels, resulting in a nonlinear transfer function of the ADC. This introduces harmonics in the output. Another source to nonlinearities is the offset error voltage on the input of each comparator, which is different for each comparator due to process variations. However, if DEM is applied, the spurious tones in the output can be suppressed.

Another error source in flash ADCs is the signal feedthrough of the input signal to the reference levels, due to the parasitic capacitance between the two comparator inputs. According to [13], the feedthrough to the worst case reference output (midpoint) is approximately

$$V_{MID} = \frac{\pi}{4} f_{IN}(R \cdot n) C_{TOT} \cdot V_{IN}, \qquad (1)$$

where n is the number of resistors of size R in the reference generator and f_{IN} is the input frequency. Hence, if R is made sufficiently small, the frequency dependent part of V_{MID} can be made sufficiently small, thereby reducing the effect of the signal feedthrough. However, R should not be too small, since the matching of the resistors then becomes poorer and the power consumption of the reference generator becomes unnecessarily high.

3. PROPOSED FLASH ADC ARCHITECTURE

In [7] the DEM is introduced by adding three switches at each reference level of the reference generator, as illustrated in Figure 2. Two of the switches are connected to the reference generator supply and the third is connected between adjacent resistors. Hence, the reference generator now consists of a number of resistors and switches in series.

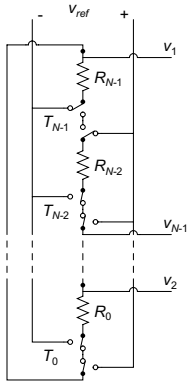


Figure 2: DEM for flash ADC, proposed in [7].

Since the resistance of the reference generator should be small enough to reduce the feedtrough of the input signal, the switches must be designed to have a low resistance. For a MOS transistor switch this means that it should be made wide. For example, in [13] the total resistance ($R_{TOT} = R \cdot n$) is 120 Ω. Since the circuit has 63 reference levels (6 bit ADC), it means that the on-resistance of each switch should be around 2 Ω, neglecting the resistors. This low on-resistance is not feasible in practice, since it would require a very wide transistor, which would consume excessive chip area and introduce excessive parasitic capacitance. Since the physical separation of each output of the reference generator is set by the pitch of the comparators, which is minimized to reduce the effects of clock and signal skew [13], this is also a reason to why the solution in [7] is only usable for low speed applications, where R_{TOT} can be made larger.

The principle of the DEM in [10] is the same as in [7]. The resistors in the reference generator are, however, replaced by the switch transistors. The switch transistors are charged by a fixed amount of charge at each sample instant, which determines the on resistance of the switch transistors. However, this circuit has the same disadvantage as the one in [7], i.e., for high speed applicatins the size is too large. The circuit is also somewhat complicated and contains ten transistors at each reference level, which introduces a large parasitic capacitance at the reference generator outputs.

Our proposal aims at removing the switch connected between adjacent resistors. According to Figure 3, we use twice the amount of resistors and connect the two resistor ladders in a circular ladder. The supply voltages to the reference generator are then connected to a pair of nodes of the resistor net that divides it into two ladders with equal resistance. A random generator controls which nodes to connect to via a switch-net (as shown in Figure 3).

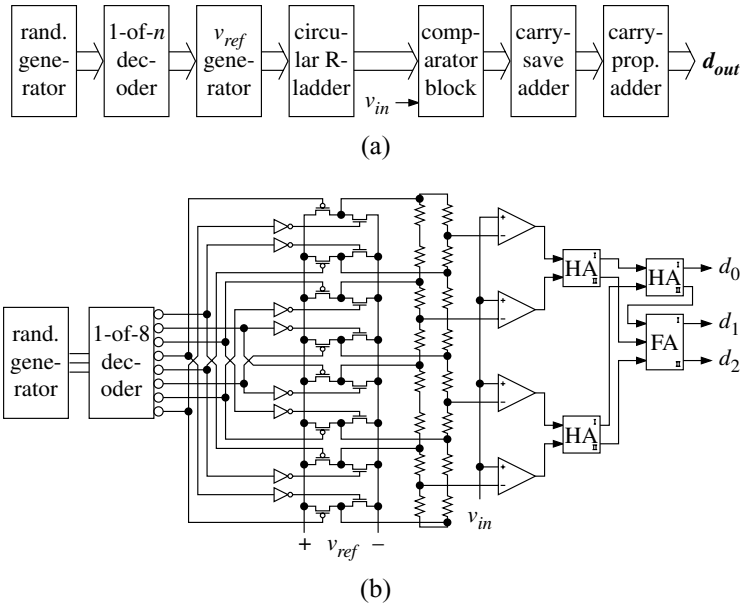


Figure 3: Block diagram (a) of proposed DEM flash ADC and the schematic (b) of our proposed DEM flash ADC (five quantization levels).

The random generator generates a random binary number that is decoded to a one, on one of the outputs of the 1-of-8 decoder. This determines where, on the circular resistor ladder, v_{ref+} and v_{ref-} are connected, which determines each of the reference voltages. The advantage of this solution is that the total resistance of the resistor ladder (R_{TOT}) still can be chosen sufficiently low to meet the requirements on input signal feedtrough, which is not the case in [7] and [10]. Hence, using our approach the circuit should be able to work at higher frequencies.

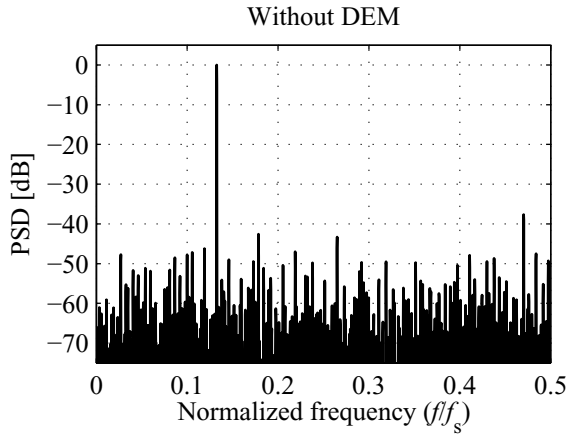
There is one major drawback with introducing DEM to a flash ADC, using a conventional thermometer to binary decoder. To connect the comparator connected to the lowest reference voltage to the decoder input with the lowest weight, etc., a switch net has to be added between the comparators and the decoder. This approach, however, cancels the DEM effect on the offset of the comparators. Instead we suggest that the one's counter decoder approach in [11] or [12] is used. The decoder does not need to be redesigned when introducing the DEM in the reference generator, since the number of ones on the output of the comparator is still the same, only in a different order.

If v_{ref+} and v_{ref-} are connected randomly each sample, the reference voltages might have to change by a large magnitude between each sample. However, the reference generator has a certain settling time, which limits the speed of the circuit. To be able to work at even higher frequencies, we suggest that the random generator is replaced by an up/down counter and each sample randomize whether it should count up or down. Hence, the reference voltages only have to change by a magnitude equal to one LSB each sample, which improves the speed of the circuit. We refer to this as restricted DEM.

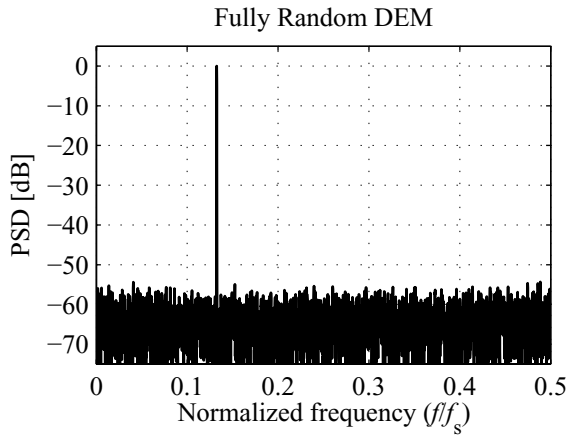
4. SIMULATION RESULTS

A Matlab model of ourproposed DEM architecture has been developed. Results from simulations of the model are shown in Figure 4. An uncertainty in the resistor values of the reference generator is included, as well as the offset of the comparators. They are considered to be Gaussian distributed with a standard deviation of σ_R = 10 % and $\sigma_{V_{os}}$ = 15 mV, respectively. The reference voltage v_{ref} is 1 V.

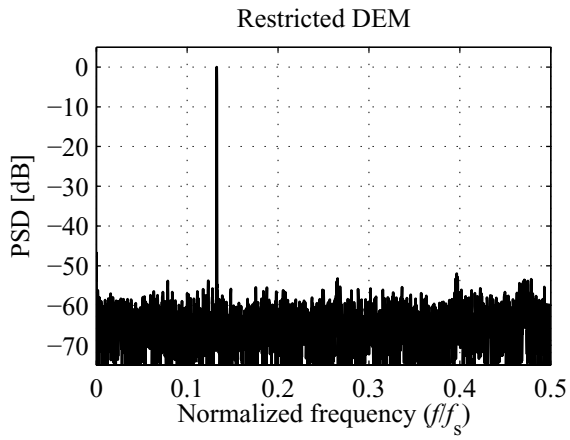
Figure 1(a) shows the spectrum when DEM is not applied. Figure 1(b) shows the spectrum when applying fully random DEM. This plot illustrates very well the fact that the spurious tones are removed and the noise floor raised. However, as mentioned earlier, this might not be a viable approach due to the settling time of the reference voltages. The spectrum of the restricted DEM is shown in Figure 1(c). This approach only moves the reference voltage supplies by one step in the resistor ladder, where the direction of the step is the randomized parameter. Hence, each reference voltage only changes by a magnitude corresponding to one LSB each sample. The time it takes for the reference voltage to settle is thereby minimized. From Figure 1(c) we conclude that the restricted DEM approach reduces the spurious tones to a large extent compared with not using DEM, and that it is almost as efficient as the fully random DEM.



(a)



(b)



(c)

Figure 4: Output spectrum without DEM (a), with fully random DEM (b) and restricted DEM (c). N=6 bits, σ_R=10 % and σ_{Vos}=15 mV.

5. CONCLUSIONS

Our proposed DEM flash ADC is more suitable for high speed applications and the complexity of our proposed circuit is lower than compared to prior solutions. Our proposed circuit has been modeled in Matlab and from the simulation results it can be seen that the restricted DEM is almost as efficient as the fully random DEM. From this we conclude that to further improve the speed performance of the circuit, the restricted DEM should be used.

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